



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/379,702	08/24/1999	HISASHI OHTANI	07977/093002	1613
20985	7590	07/06/2006	EXAMINER	
FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			LEE, EUGENE	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 07/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

MAILED
JUL 10 2006
GROUP 2800

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/379,702
Filing Date: August 24, 1999
Appellant(s): OHTANI ET AL.

John F. Hayden
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/6/04.

(1) *Real Party in Interest*

A statement identifying the real party in interest is contained in the brief.

(2) *Related Appeals and Interferences*

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) *Status of Claims*

The statement of the status of the claims contained in the brief is correct.

(4) *Status of Amendments After Final*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) *Summary of Invention*

The summary of invention contained in the brief is correct.

(6) *Issues*

The appellant's statement of the issues in the brief is correct.

Art Unit: 2815

(7) *Grouping of Claims*

The rejection of claims 45-64 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) *Claims Appealed*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) *Prior Art of Record*

5,315,132	Yamazaki	5-1994
5,396,084	Matsumoto	3-1995

(10) *Grounds of Rejection*

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 45 thru 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki 5,315,132 in view of Matsumoto 5,396,084. Yamazaki discloses (see, for example,

Art Unit: 2815

FIG. 3) a thin film transistor (semiconductor device) comprising a crystalline semiconductor layer (crystalline semiconductor island) 2, substrate 1, source region 5S, drain region 5D, channel region (channel formation region) 5D, gate insulating film 3, and gate electrode 5G. The gate insulating film comprises a first insulating film with a side aligned with a side of the crystalline semiconductor layer 2. Yamazaki does not disclose a gate insulating film comprising a second insulating film extending beyond an edge of the first insulating film. However, Matsumoto discloses (see, for example, FIG. 1) a thin film semiconductor device comprising a thin film transistor 2 in a matrix circuit portion of a liquid crystal display device wherein the thin film transistor comprises an interlayer insulating film (second insulating film) 19 on top of gate insulating film 14, and that blanket extends across the thin film transistor. In column 4, lines 65-68, and column 4, lines 47-49, Matsumoto discloses the interlayer insulating film and gate insulating film consisting of silicon oxide or silicon nitride. In column 5, lines 21-56, Matsumoto teaches that the gate insulating film in the matrix circuit portion will increase the on-voltage and suppress the increase in current consumption. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the interlayer insulating film (second insulating film) 19 of Matsumoto on top of the gate insulating film 3 of Yamazaki in order to form a liquid crystal display device wherein the matrix circuit portion has increased on-voltage and suppresses the increase in current consumption.

Regarding claims 50-59, these claims contain product-by-process limitations (i.e. formed by irradiating a laser light) that add no structural limitations to the applicant's claims.

Regarding claims 60-64, see column 6, line 13 wherein Yamazaki states the substrate as being quartz glass (glass substrate).

Product-by-Process Limitations

While not objectionable, the Office reminds Applicant that “product by process” limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or *otherwise*. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

(11) Response to Argument

In response to the appellant’s argument (on page 2, last paragraph) that the Examiner’s conclusion of obviousness is based upon an impermissible hindsight reconstruction, it must be recognized that any judgment on obviousness is in any sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the invention was made, and does not include knowledge gleaned only from the Applicant’s disclosure, such a reconstruction is proper. *In re McLaughlin*, 443 F. 2d 1392; 170 USPQ 209 (CCPA 1971).

In this case, Matsumoto clearly discloses (see column 5, lines 21-56 and FIG. 1) that by combining an interlayer insulating film 19 with a gate insulating film 14, one can structurally create a thicker gate insulating film in a matrix circuit portion for a liquid crystal device. The thicker gate insulating film increases the distance between the gate electrode and channel region, thereby increasing the on voltage and suppressing an increase in current consumption. Therefore, Matsumoto provides the knowledge within the level of ordinary skill at the time of invention, and hence the reconstruction of Yamazaki in view of Matsumoto is proper.

On page 3, second paragraph of the appeal brief, the appellant mentions the thicknesses of the gate insulating film and interlayer insulating film. However, the thicknesses of the individual films are not of issue in this case since the specific thicknesses are not stated in the appellant's claims.

The appellant's argument on page 4, first paragraph that a person of ordinary skill in the art would have been much more likely to have taken the first approach, than the fourth approach, this argument is not persuasive. The approaches cited by the applicant are methods and, therefore, not an issue with respect to the claimed invention. This is because the invention, as set forth in the claims, is clearly directed towards apparatus. However, even if the method used to form the structure of Yamazaki in view of Matsumoto was critical, the likeliness to choose one approach over another is based on appellant's speculation. This is because the appellant has provided no factual evidence, and more importantly, it does not preclude the fact that Matsumoto has provided a clear motivation (increase the on-voltage and suppress an increase in current consumption) to include an interlayer insulating film over Yamazaki's gate insulating film 3.

Art Unit: 2815

It should also be noted that the first insulating film having a side aligned with a side of the crystalline semiconductor island is a feature that is not stated as critical in the applicant's disclosure. Nowhere in the specification does the applicant state that the side aligned with a side of the crystalline semiconductor island is critical to the operation of the applicant's device. Instead, the applicant's invention is directed towards a different purpose, a silicon film which is crystallized by the catalytic action of a metal element.

For the above reasons, it is believed that the rejections should be sustained.

Application/Control Number: 09/379,702
Art Unit: 2815

Page 8

Respectfully submitted,


Eugene Lee
December 16, 2004



Conferees

OC, 502
Tom Thomas *T T*
AU 2815

OC
Olik Chaudhuri
AU 2823


Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800

FISH & RICHARDSON, PC
4350 LA JOLLA VILLAGE DRIVE
SUITE 500
SAN DIEGO, CA 92122